

# Modeling and measurements of novel high $k$ monolithic transformers

Aly H. Aly, Badawy Elsharawy

Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287-7206

**Abstract** This paper presents modeling and measurements of a novel monolithic transformer with high coupling  $k$  and quality factor  $Q$  characteristics. The present transformer utilizes a Z-shaped multi-layer metalization to increase  $k$  without sacrificing  $Q$ . The new transformer has been fabricated using Motorola 0.18 micron copper process. A simple 2-port lumped circuit model is used to model the new design. Experimental data shows a good agreement with predicted data obtained from an HFSS software simulator. An increase of about 10% in mutual coupling and 15% in  $Q$  has been achieved. For a modest increase in  $k$  of about 5%,  $Q$  can be increased by up to 20%.

## I. INTRODUCTION

Applications such as high linearity differential amplifiers for CDMA (code division multiplexing) and balanced mixers require transformers or baluns. An approach to realize baluns [1] or transformers is to use spirals to minimize the required chip space. Previous research [2] shows that the quality factor of the 2-port transformer is higher than the quality factor of the inductor by a factor of  $(1+k)$  where  $k$  is the coupling coefficient. However, if integrated on silicon transformer still suffer from lower  $Q$ -factor. The major problem in designing transformers is that they are extremely sensitive to variation of process parameters. The operation of a passive transformer is based upon the mutual inductance between two or more windings which is proportional to the coupling factor  $k$ . The ideal value of  $k$  is equal to one, however for most practical monolithic transformers;  $k$  exhibits values between 0.3-0.9. On-chip transformers can be realized in different configuration. Conventional configurations include interleaved and stacked transformers. These configurations offer varying trade-offs among the self-inductance and series resistance, mutual coupling coefficient, resonance frequency, symmetry and area. For example, interleaved transformer offer higher resonance frequency, low self-inductance, but medium coupling while the stacked transformers offer the high coupling but at the expense of

reducing quality factor and self-resonance frequency. Stacked transformers have typically high self-inductance and parasitic capacitances [2]. Coupling and  $Q$  can simultaneously be increased by increasing the metal thickness. Our early work on multi-layer transformers [2] connected in parallel had resulted in a relatively small increase in coupling (less than 5%) and  $Q$ .

This paper presents a novel transformer configuration to give higher coupling coefficients and higher quality factor. Two layers of metalization are connected by an array of edge vias to form an interleaved transformer with a stacked overlap as shown in Fig. 1. Section II presents modeling and experimental results of a set of fabricated transformers and the paper is concluded in section IV.

## II. RESULTS

To illustrate the concept of the Z-topology, Fig.1 shows the metalization of the present transformer. The primary and secondary winding are implemented on two layers with the lower metal radially shifted inward or outward from the top metal by slightly less than metal width. As mentioned above, the two metalization are connected through an array of edge vias. This Z shaped conductor will alter the flux lines for better coupling between adjacent line and less fringe fields, which reduce the winding self-inductance and increase the mutual inductance. The increased cross section of the conductor will reduce their ohmic resistance and increase  $Q$ .

To examine the proposed concept, different on-silicon two-port transformers were fabricated using Motorola 0.18-micron process. Due to limited wafer space, the conductor width was set to five microns and spacing to one micron. A micro photo image of the five and four turns transformers after fabrication is shown in Fig. 2.



TABLE I  
LUMPED CIRCUIT MODEL PARAMETER VALUES FOR MEASURED 2-PORT TRANSFORMER

N	2-Port transformer						
	Ls(nH)	K	Rs (ohm)	Cc(fF)	Cox(fF)	Rsi (ohm)	Csi (fF)
<b>5 turns (Normal)</b> (180 microns X 180 microns)	4.8413	0.7743	27.79	15.4	239	7.67	19.53
<b>5 turns (Z-SO)</b> (180 microns X 180 microns)	4.79	0.88	13.58	54.43	560	8.34	15.39
<b>5 turns (Z-SI)</b> (180 microns X 180 microns)	4.68	0.84	12.66	61	576	8.7	19
<b>4 turns (Normal)</b> (158 microns X 158 microns)	3.135	0.76	23.3	10.3	157.53	9	20
<b>4 turns (Z-SO)</b> (158 microns X 158 microns)	3.04	0.835	12.4	48.64	420	9	15
<b>4 turns (Z-SI)</b> (158 microns X 158 microns)	2.73	0.827	11.8	53	442.4	8.99	15.93

The 8510C network analyzer and Cascade Microtech coplanar ground-signal-ground probes were used to measure the S-parameters of the transformers. During the measurements, the substrate was grounded at the back using the testing chuck. The shunt parasitics of the pads in the testing structures were also measured. Fig.3 shows the measured, simulated, S-parameters of the planar transformer. The simulation has been generated using HFSS software package [5]. Good agreement can be observed between the simulated and measured parameters.

The S-parameters were used to generate an equivalent circuit model as shown in Fig.4. Part 1 of the circuit models is the parasitics introduced by the pads. Part 2 of the circuit model is the transformer itself. The primary and secondary winding are mutually coupled by a factor  $k$ . Using ADS software package [6], an extraction algorithm is performed to solve for circuit parameters. The circuit includes the conductor resistance  $R_s$ , the self-inductance  $L_s$ , the inter-winding capacitance  $C_c$ , oxide capacitance  $C_{ox}$ , and substrate equivalent resistance  $R_{si}$  and capacitance  $C_{si}$ . Table 1 shows the extracted values for the equivalent circuit model. Two types of the Z-transformer are presented with opposite shift directions. The equivalent circuit was optimized to match the experimental data.

Table I shows that the Z-transformer has lower resistance and self-inductance for the same number of turns. The coupling coefficient  $k$  increases consistently

with increasing the number of turns and is confirmed to be higher for the Z-configuration. This is however, at the expense of parasitic capacitances, which increased significantly. Figure 3 shows also the S-parameters of the equivalent circuit compared to both measured and simulated data.

To show the impact of the Z-configuration, Fig.5 shows the measured S-parameters for interleaved and the Z-configuration with both inward and outward shift. Generally,  $S_{12}$  and  $S_{21}$  of the Z-transformers are about 3 dB higher than the interleaved transformer. Higher  $S_{21}$  and  $S_{12}$  indicate tighter transformer coupling as discussed earlier. The differential quality factor  $Q$ , is given by [2].

$$Q_{diff} = \frac{\omega(1+k)L_s \left( 1 - \left( \frac{\omega}{\omega_{srf,diff}} \right)^2 \right)}{R_s} \left( 1 - \frac{R_s^2 C_{ox}}{(1+k)L_s} \right)$$

And

$$\omega_{srf,diff} = \frac{1}{\sqrt{(1+k)L_s C_{ox}}} \left( 1 - \frac{R_s^2 C_{ox}}{(1+k)L_s} \right)^{\frac{1}{2}}$$

where  $\omega$  is the radian frequency. Fig.6 shows the quality factor  $Q$  for different configurations versus frequency. As shown in the figure,  $Q$  of the Z transformers is higher than the interleaved transformer by up to 15%. Simultaneously, the coupling factor increased by 10%. Note that, there is decrease in the self-resonance frequency. Comparing the five turns interleaved to the four turns Z-transformer shows for the same resonant frequency it is possible to obtain higher coupling and higher  $Q$ . In this case  $Q$  is higher by up to 20% and  $k$  is higher by about 5% and the chip area is reduced by 25%. Increasing the metal width and adding the poly-patterned feature [7] can be used for further optimization of  $Q$ ,  $k$ , and  $f_r$ .

### III. FIGURES

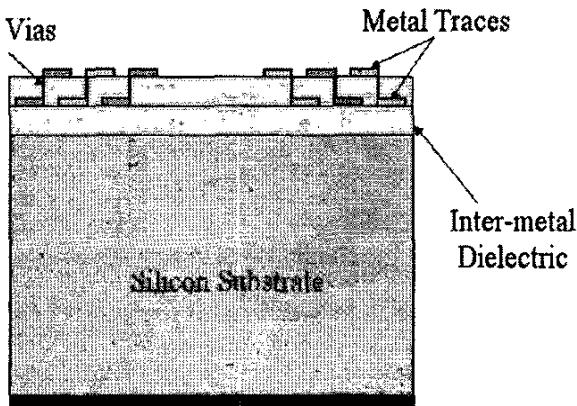


Fig.1 Backside metalization of Z-transformer

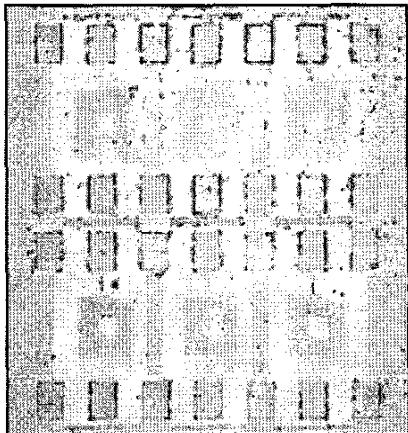
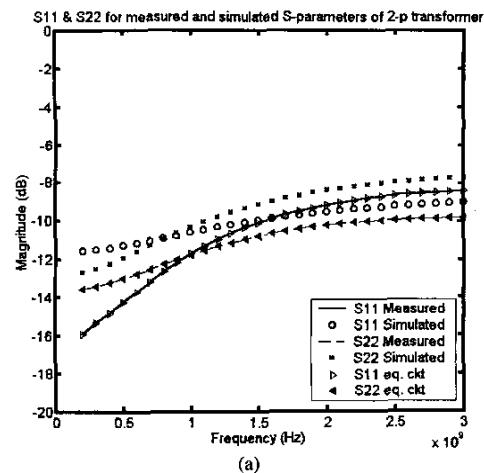
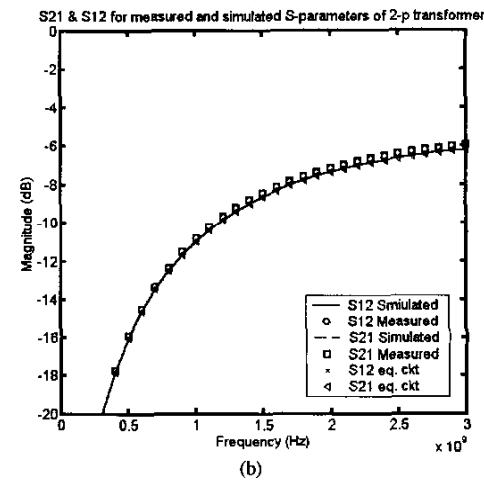


Fig.2 Micro photo image of 2-port transformers using Mot. 0.18-micron process



(a)



(b)

Fig.3 Measured, simulated, and equivalent circuit S-parameters of the 2-port transformer.

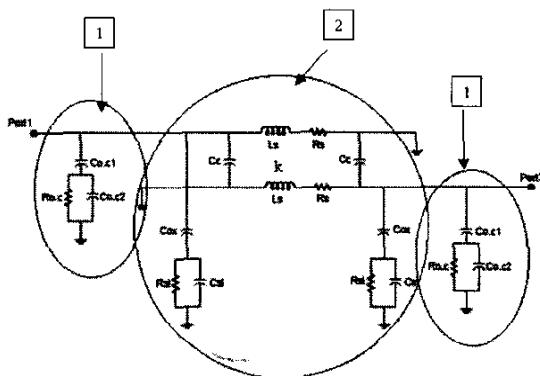
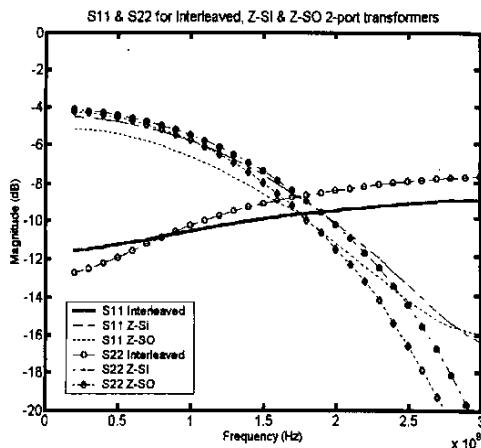
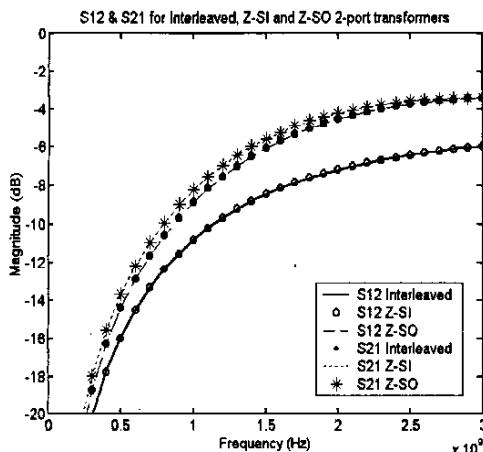


Fig.4 Equivalent circuit model for 2-port transformer include the pad effect



(a)



(b)

Fig.5 Measured S-parameters for Interleaved, Z-SI and Z-SO 2-port transformers

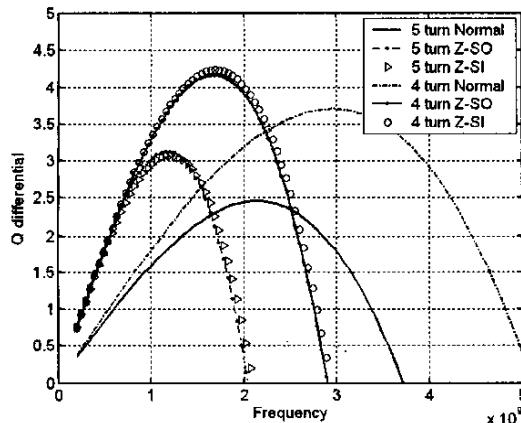


Fig.6 Quality factor for different 2-port transformers

#### IV. CONCLUSION

In this paper, a novel transformer configuration is introduced. Experimental results show promising performance of the introduced devices. The structures were simulated using HFSS program. Equivalent circuit models were presented. Simulation and experimental results show an increase of the quality and coupling factors of the proposed transformer as compared to the conventional transformers

#### ACKNOWLEDGEMENT

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